Ternarylogic

Dear IP Professional,

This document contains a list of issued patents and pending patent applications assigned to Ternarylogic LLC of Morristown, NJ as of March 2016. The status of the portfolio still changes as the USPTO continues to allow and issue patents in the portfolio and new applications are filed.

A copy of this document can be downloaded from www.ternarylogic.com/portfolio.pdf. The document has live links to the USPTO database to make review easier.

Those who want to obtain a patent or application in PDF format are referred to www.pat2pdf.org which allows downloading a patent or patent application in PDF format. Just enter the patent or patent publication number into the search window.

Many applications are still alive, even after issuance, by filing of continuations and continuations-in-part. Please, check USPTO PAIR for case histories.

This document is provided "as is" for your review. Please, contact us at admin@ternarylogic.com if you are interested in obtaining a license. Please note that some patents contain errors in the claims. Some claims wrongly exclude binary configurations. It is strictly the reader's responsibility to decide if a claim is infringed. Please check a patent's case history in PAIR when in doubt.

The subject matter of the portfolio

The subject matter of the portfolio is related to non-binary switching and applications thereof. The portfolio covers a range of subjects that includes:

- basic components such as n-state switches, inverters and memories;
- non-binary and binary Linear Feedback Shift Register applications;
- binary and non-binary self synchronizing scramblers/descramblers;
- machine arithmetic;
- encryption;
- error-correction methods and apparatus;
- secure unlocking of devices; and
- general applications in finite field arithmetic over GF(n).

How to access the portfolio

Please click on a specific patent number or patent application number to open a related web site at the U.S. Patent and Trademark Office (USPTO).

Contact us

Ternarylogic LLC
admin@ternarylogic.com

Issued patents

46	9,298,423		Methods and systems for determining characteristics of a sequence of n-state symbols
45	9,218,158		N-Valued Shift Registers with Inverter Reduced Feedback Logic Functions
44	9,203,438		Error correction by symbol reconstruction in binary and multi-valued cyclic codes
43	9,203,436		Error correction in multi-valued (p,k) codes
42	9,100,166		Method and apparatus for rapid synchronization of shift register related symbol sequences
41	8,832,523		Multi-state symbol error correction in matrix based codes
40	8,817,928		Method and apparatus for rapid synchronization of shift register related symbol sequences
39	8,645,803		Methods and systems for rapid error correction by forward and reverse determination of coding states
38	8,589,466		Ternary and multi-value digital signal scramblers, descramblers and sequence generators
37	8,577,026		Methods and apparatus in alternate finite field based coders and decoders
36	8,374,289		Generation and detection of non-binary digital sequences
35	8,364,977		Methods and systems for processing of n-state symbols with XOR and EQUALITY binary functions
34	8,345,873		Methods and systems for N-state signal processing with binary devices
33	8,225,147		Multi-valued scrambling and descrambling of digital data on optical disks and other storage media
32	8,209,370		Multi-value digital calculating circuits, including multipliers
31	8,201,060		Methods and systems for rapid error correction of Reed-Solomon codes
30	8,180,817		Encipherment of digital sequences by reversible transposition methods
29	8,149,143		Data encryption and decryption with a key by an N-state inverter modified switching function
28	8,103,943		Symbol reconstruction in Reed-Solomon codes
27	8,046,661		Symbol error correction by error detection and logic based symbol reconstruction
26	7,930,331		Encipherment of digital sequences by reversible transposition methods
25	7,924,176		N-state ripple adder scheme coding with corresponding N-state ripple adder scheme decoding
24	7,877,670		Error correcting decoding for convolutional and recursive systematic convolutional encoded sequences
23	7,865,807		Multi-valued check symbol calculation in error detection and correction
22	7,865,806		Methods and apparatus in finite field polynomial implementations

21	7,864,087		Methods and systems for modifying the statistical distribution of symbols in a coded message
20	7,864,079		Ternary and higher multi-value digital scramblers/descramblers
19	7,782,089		Multi-state latches from n-state reversible inverters
18	7,772,999		N-state ripple adder scheme coding with corresponding n-state ripple adder scheme decoding
17	7,725,779		Multi-valued scrambling and descrambling of digital data on optical disks and other storage media
16	7,696,785		Implementing logic functions with non-magnitude based physical phenomena
15	7,659,839		Methods and systems for modifying the statistical distribution of symbols in a coded message
14	7,656,196		Multi-state latches from n-state reversible inverters
13	7,643,632		Ternary and multi-value digital signal scramblers, descramblers and sequence generators
12	7,580,472		Generation and detection of non-binary digital sequences
11	7,562,106		Multi-value digital calculating circuits, including multipliers
10	7,548,092		Implementing logic functions with non-magnitude based physical phenomena
9	7,505,589		Ternary and higher multi-value digital scramblers/descramblers
8	7,487,194		Binary and n-valued LFSR and LFCSR based scramblers, descramblers, sequence generators and detectors in Galois configuration
7	7,397,690		Multi-valued digital information retaining elements and memory devices
6	7,365,576		Binary digital latches not using only NAND or NOR circuits
5	7,355,444		Single and composite binary and multi-valued logic functions from gates and inverters
4	7,277,030		Sequence detection by multi-valued coding and creation of multi-code sequences
3	7,218,144		Single and composite binary and multi-valued logic functions from gates and inverters
2	7,064,684		Sequence detection by multi-valued coding and creation of multi-code sequences
1	7,002,490		Ternary and higher multi-value digital scramblers/descramblers

One is cautioned that the issued patents cover inventions as provided in the claims. The title of a patent may refer to a parent patent of which it is a continuation. Furthermore, claims in an issued patent may have mistakes that are corrected by a Certificate of Correction. Furthermore, additional aspects may be claimed in continuation applications that have not yet been issued. Please review a patent's case history in the USPTO PAIR website for details.

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Ternarylogic LLC will try to update this document on a regular basis. However, no guarantee is provided on its correctness or its current status. Only the USPTO database provides the most current data. One is advised to check this database on the status on any of the patents and patent applications related to Ternarylogic LLC.

PUBLISHED Patent Applications

20150310680	Method and Apparatus for Wirelessly Activating a Remote Mechanism
20150160922	N-Valued Shift Registers with Inverter Reduced Feedback Logic Functions
20140321585	Method and Apparatus for Rapid Synchronization of Shift Register Related Symbol Sequences
20140281761	Reversible corruption of a digital medium stream by multi-valued modification in accordance with an automatically generated mask
20140055290	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders
20140032623	Methods and Systems for Determining Characteristics of a Sequence of n-state Symbols
20130230172	Novel binary and n-state Linear Feedback Shift Registers (LFSRs)
20120233527	Methods and Systems for Rapid Error Location in Reed-Solomon Codes
20120170738	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders
20110293062	Method and Apparatus for Rapid Synchronization of Shift Register Related Symbol Sequences (rapid synchronization of binary and n-state LFSRs based on received symbols)
20110276854	Methods and Systems for Rapid Error Correction by Forward and Reverse Determination of Coding States (fast RS decoding of long sequences with single errors)
20110214038	Methods and Systems for Rapid Error Correction of Reed-Solomon Codes (one of several applications that perform 'real-time' error location in RS code words)
20110182423	Data Encryption and Decryption with a Key by an N-state Inverter Modified Switching Function
20110064214	Methods and Apparatus in Alternate Finite Field Based Coders and Decoders (applies novel adders and multiplications over GF(n))
20100322414	TERNARY AND HIGHER MULTI-VALUE DIGITAL SCRAMBLERS/DESCRAMBLERS (**issued**)

20100299579	Methods and Systems for Error-Correction in Convolutional and Systematic Convolutional Decoders in Galois Configuration
20100271243	N-State Ripple Adder Scheme Coding with Corresponding N-State Ripple Adder Scheme Decoding (**issued**. Despite title, claims novel Feistel-like networks)
20100211803	Multi-Valued Scrambling and Descrambling of Digital Data on Optical Disks and Other Storage Media (Despite title, claims rapid synchronization of sequences)
20100180097	Generation and Self-Synchronizing Detection of Sequences Using Addressable Memories
20100164548	Implementing Logic Functions With Non-Magnitude Based Physical Phenomena
20100109922	Methods and Systems for Modifying the Statistical Distribution of Symbols in a Coded Message (**issued**)
20100085802	Multi-State Latches From n-State Reversible Inverters (**issued**)
20090285326	Generation and Detection of Non-Binary Digital Sequences (Despite title, claims novel correlation methods and apparatus)
20090234900	Multi-Value Digital Calculating Circuits, Including Multipliers
20090172501	Multi-State Symbol Error Correction in Matrix Based Codes
20090146851	N-State Ripple Adder Scheme Coding with Corresponding N-State Ripple Adder Scheme Decoding (**issued**)
20090138535	Novel Binary and n-State Linear Feedback Shift Registers (LFSRs)
20090128190	Implementing Logic Functions with Non-Magnitude Based Physical Phenomena
20090092250	Methods and Systems for N-State Signal Processing with Binary Devices
20090077151	Multi-Input, Multi-State Switching Functions and Multiplications
20090060202	Ternary and Higher Multi-Value Digital Scramblers/Descramblers
20090045988	Methods and Systems for Modifying the Statistical Distribution of Symbols in a Coded Message (**issued**)
20080244274	Methods and Systems for Processing of n-State Symbols with XOR and EQUALITY Binary Functions
20080180987	Multi-State Latches From n-State Reversible Inverters (**issued**)
20080111583	IMPLEMENTING LOGIC FUNCTIONS WITH NON-MAGNITUDE BASED PHYSICAL PHENOMENA (**issued**)
20080104479	Symbol Error Correction by Error Detection and Logic Based Symbol Reconstruction
20080040650	Symbol Reconstruction in Reed-Solomon Codes (**issued**)
20080016432	Error Correction in Multi-Valued (p,k) Codes
20080016431	ERROR CORRECTION BY SYMBOL RECONSTRUCTION IN BINARY AND MULTI-VALUED CYCLIC CODES

20070258516	MULTI-VALUED CHECK SYMBOL CALCULATION IN ERROR DETECTION AND CORRECTION (**issued**)
20070239812	Binary And N-Valued LFSR And LFCSR Based Scramblers, Descramblers, Sequence Generators and Detectors In Galois Configuration (**issued**)
20070226594	ERROR CORRECTING DECODING FOR CONVOLUTIONAL AND RECURSIVE SYSTEMATIC CONVOLUTIONAL ENCODED SEQUENCES (**issued**)
20070208796	METHODS AND APPARATUS IN FINITE FIELD POLYNOMIAL IMPLEMENTATIONS (**issued**)
20070152710	SINGLE AND COMPOSITE BINARY AND MULTI-VALUED LOGIC FUNCTIONS FROM GATES AND INVERTERS (**issued**)
20070110229	Ternary and Multi-Value Digital Signal Scramblers, Descramblers and Sequence of Generators (**allowed**)
20070098160	SCRAMBLING AND SELF-SYNCHRONIZING DESCRAMBLING METHODS FOR BINARY AND NON-BINARY DIGITAL SIGNALS NOT USING LFSRs
20070088997	GENERATION AND SELF-SYNCHRONIZING DETECTION OF SEQUENCES USING ADDRESSABLE MEMORIES
20070071068	ENCIPHERMENT OF DIGITAL SEQUENCES BY REVERSIBLE TRANSPOSITION METHODS (**allowed**)
20070005673	The Creation and Detection of Binary and Non-Binary Pseudo-Noise Sequences Not Using LFSR Circuits
20060282607	Binary digital latches not using only NAND or NOR circuits (**issued**)
20060187092	Sequence detection by multi-valued coding and creation of multi-code sequences (**issued**)
20060164883	Multi-valued scrambling and descrambling of digital data on optical disks and other storage media (**issued**)
20060031278	Multi-value digital calculating circuits, including multipliers (**issued**)
20050278661	Multi-valued digital information retaining elements and memory devices (**issued**)
20050265463	Sequence detection by multi-valued coding and creation of multi-code sequences (**issued**)
20050194993	Single and composite binary and multi-valued logic functions from gates and inverters (**issued**)
20050185796	Ternary and multi-value digital signal scramblers, descramblers and sequence generators (**issued**)
20050184888	Generation and detection of non-binary digital sequences (**issued**)
20050084111	Ternary and higher multi-value digital scramblers/descramblers
20050053240	Ternary and higher multi-value digital scramblers/descramblers